Abstract

A signal processing circuit and method in which a given signal, e.g., a receive data clock associated with a first chip and generated by a deserializer circuit, is synchronized with another signal, e.g., a clock signal from a second chip which is asynchronous with the receive data clock. The circuit may include first, second and third processing circuits, each of which performs a sampling function on a corresponding one of an early version, a middle version and a late version of the given signal, utilizing the clock signal to which the given signal is to be synchronized. A logic circuit coupled to outputs of each of the first, second and third processing circuits generates a control signal indicative of the presence or absence of a desired relationship, e.g., a desired phase relationship, between the clock signal and the first, second and third versions of the given signal. A selection circuit, e.g., a set of multiplexers, is responsive to the control signal to alter the phase relationship between the clock signal and the first, second and third versions of the given signal if the control signal indicates the absence of the desired relationship. The logic and selection circuits may be configured as part of a feedback control loop which automatically maintains the desired relationship.